F384/F640

Uncooled Thermal Imaging Module

User Expansion Component Manual

V1.0.1

Version History

Version	Date	Description
V1.0.0	2024-07	Initial release
V1.0.1	2024-09	Add descriptions on user expansion component 07

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1 User Expansion Component 01

The 01 user expansion component is compatible with 384 and 640 thermal imaging modules. It includes 5 sockets, as shown in Figure 1.1. This user expansion component supports BT656/BT1120 output, UART (or RS232), RS485, 1 channel analog video, external synchronization, alarm, motor control, temperature sensor, and other interfaces. The interface definitions are as shown in the table below. A standard wiring cable is included. For specific details, please refer to sections 1.1 to 1.5.

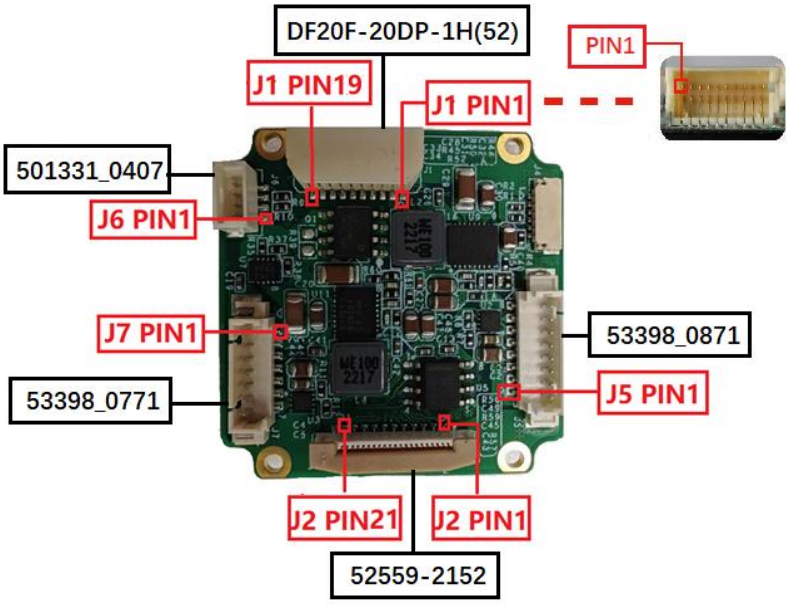

Figure1.1 Expansion Component 01

1.1 Zoom Motor Control Socket

The power socket uses the MOLEX 53398-0771 7-pin connector, providing interfaces for the lens zoom motor drive, zoom potentiometer drive, and signal collection. The socket interface definitions are shown in Table 1.1.

Table1.1 The Interface Definition of MOLEX 53398-0771

PIN NO.	PIN Name	Type	Description
1	+12V_OUT	Power	Power Output 12V
2	GND	Power	Ground of Power
3	ZOOM_VOLTAGE	Input	Feedback of Zoom Potentiometer
4	/	/	/
5	/	/	/
6	ZOOM_MOTOR+	In/Out	Motor Driver In/Out
7	ZOOM_MOTOR-	In/Out	Motor Driver In/Out

1.2 Focus Motor Control Socket

The focus motor control socket uses the MOLEX 53398-0871 8-pin connector, providing interfaces for the lens focus motor drive, focus potentiometer drive, and signal collection. The socket interface definitions are shown in Table 1.2.

Table1.2 The Interface Definition of 53398-0871

PIN NO.	PIN Name	Type	Description
1	+12V_OUT	Power	Power Output 12V
2	GND	Power	Ground of Power
3	FOCUS_VOLTAGE	Input	Feedback of Focusing potentiometer
4	/	/	/
5	/	/	/
6	FOCUS_MOTOR+	In/Out	Motor Driver In/Out(12V)
7	FOCUS_MOTOR-	In/Out	Motor Driver In/Out
8	/	/	/

1.3 Digital Video Output Socket

The digital video output socket uses the MOLEX 52559-2152 21-pin socket, supporting BT.601, BT.1120, and LVCMOS digital video output. The socket interface definitions are shown in Table 1.3.

Table1.3 The Interface Definition of MOLEX 52559-2152

PIN NO.	PIN Name	Type	Description
1	DV1	Output	BT.656/BT.1120/LVCMOS digital signal1
2	DV0	Output	BT.656/BT.1120/LVCMOS digital signal 0
3	DV3	Output	BT.656/BT.1120/LVCMOS digital signal 3
4	DV2	Output	BT.656/BT.1120/LVCMOS digital signal 2
5	DV5	Output	BT.656/BT.1120/LVCMOS digital signal 5
6	DV4	Output	BT.656/BT.1120/LVCMOS digital signal 4
7	DV7	Output	BT.656/BT.1120/LVCMOS digital signal 7
8	DV6	Output	BT.656/BT.1120/LVCMOS digital signal 6
9	DV9	Output	BT.1120/LVCMOS digital signal 9
10	DV8	Output	BT.1120/LVCMOS digital signal 8
11	DV11	Output	BT.1120/LVCMOS digital signal 11
12	DV10	Output	BT.1120/LVCMOS digital signal 10
13	DV13	Output	BT.1120/LVCMOS digital signal 13
14	DV12	Output	BT.1120/LVCMOS digital signal 12

15	DV15	Output	BT.1120 digital signal 15
16	DV14	Output	BT.1120 digital signal 14
17	GND	Power	Ground of power
18	DV_VSYNC	Output	Frame valid signal
19	DV_HSYNC	Output	Row valid signal
20	GND	Power	Power Ground
21	DV_CLK	----	Clock signal

1.4 Temperature Sensor Socket

The temperature sensor socket uses the MOLEX 501331-0407 4-pin socket, providing the lens temperature sensor interface. The socket interface definitions are shown in Table 1.4.

Table1.4 The Interface Definition of MODEX 501331_0407

PIN NO.	PIN Name	Type	Description
1	TMP_SCL	In/Out	Temperature sensor I2C CLK pin
2	TMP_SDA	In/Out	Temperature sensor I2C Data Pin
3	VCCA	Power	Temperature sensor chip power supply (+1.8V)
4	GND	Power	Power GND

1.5 Power Serial Port Socket

The power serial port uses the HRS DF20F-20DP-1H 20-pin socket, supporting 5~24V DC power supply, one analog video output interface, one RS232 serial communication interface, one RS485 serial communication interface, one UART (multiplexed with RS232) serial communication interface, four button control interfaces, one sync input/output interface, and one alarm IO output. The socket interface definitions are shown in Table 1.5.

Table1.5 The Interface Definition of HRS DF20F-20DP-1H

PIN No.	PIN Name	Type	Description
1	GND	Power	Power Ground
2	POWER_IN	Power	Power input(5~24-DC)
3	GND	Power	Power Ground
4	POWER_IN	Power	Power input(5~24-DC)
5	NULL	Input	Reserved
6	GND	Power	Power Ground
7	NULL	Output	Reserved

8	RS485-	In/Out	RS485 serial input/output interface(PT control)
9	GND	Power	Power Ground
10	RS485+	In /Out	RS485 serial input/output interface(PT control)
11	EXT_SYNC	In /Out	External synchronizing input/output interface
12	KEY1	Input	Button(C)interface
13	UART_RX/ RS232_RX	Input	UART serial input interface or RS232 input interface, the factory default is RS232
14	KEY2	Input	Button(-) interface
15	UART_TX/ RS232_TX	Output	UART serial output interface or RS232 output interface, the factory default is RS232, UART should be customized.
16	KEY3	Input	Button(+) interface
17	ALARM	Output	Alarm output IO, high-low level (3.3V)
18	KEY4	Input	Button (M) interface
19	VIDEO	Output	Analog video output interface
20	VGND	Power	Analog video ground

2. User Expansion Component 38

The user expansion component 38 is suitable for 384 and 640 uncooled infrared cores. This user expansion component contains five sockets, as shown in Figure 1.1, supporting power input, RS-485, network, alarm input/output, and audio input/output interfaces. The interface definitions are shown in the figure below.

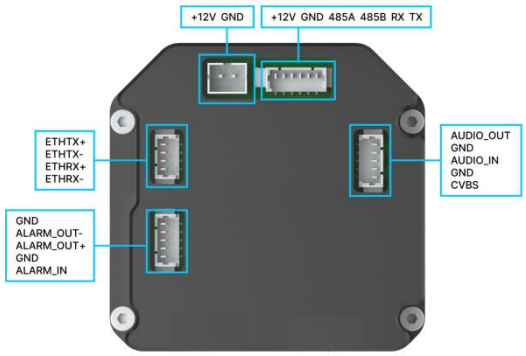

Figure 2.1 User Expansion Component 38

Additionally, when using the user expansion component 38, the adapter board includes a motor control socket, as shown in the figure below.

The motor interface definitions are shown in the table below:

Table 2.1 Definition of the Motor Control Socket on the 38 Network Board

PIN No.	PIN Name	Type	Description
1	+3.3V	Power	Power 3.3V Output
2	ZOOM_VOLTAGE	Input Signal	Zoom Potentiometer Feedback
3	GND	Power	Power GND
4	+3.3V	Power	Power 3.3V Output
5	FOCUS_VOLTAGE	Input Signal	Focus Potentiometer Feedback
6	GND	Power	Power GND
7	+1.8V	Power	Power 1.8V Output
8	TMP_SDA	In/Out	Temperature Sensor I2C Data
9	TMP_SCL	Output Signal	Temperature Sensor I2C CLK
10	GND	Power	Power GND
11	MOTOR_Z+	In/Out Signal	Motor Drive In/Out
12	MOTOR_Z-	In/Out Signal	Motor Drive In/Out
13	MOTOR_F+	In/Out Signal	Motor Drive In/Out
14	MOTOR_F-	In/Out Signal	Motor Drive In/Out

3. User Expansion Component 07

The 07 user expansion component is applicable to 384 and 640 uncooled thermal imaging modules. This user expansion component includes five sockets, as shown in Figure 3.1, and supports interfaces such as power input, RS-485, network, alarm input/output, and audio input/output. The interface definitions are shown in the figure. For detailed descriptions, refer to Sections 3.1 to 3.5.

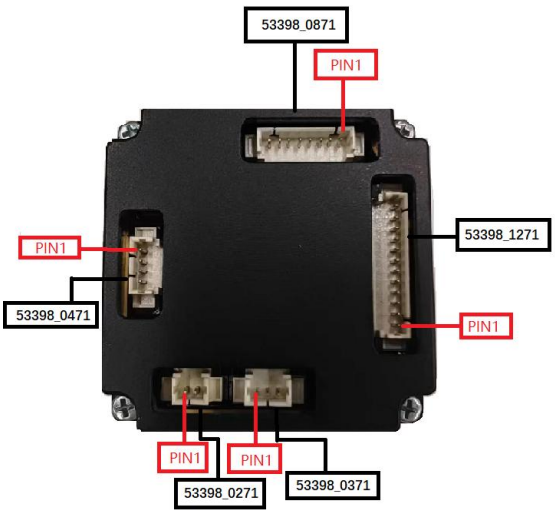

Figure 3.1 User Expansion Component 07

3.1 Speaker Out Socket

The MOLEX 2-pin connector provides audio input and output interfaces. The socket interface definitions are shown in Table 3.1.

Table 3.1 Pinout of 53398-0271 2-Pin Socket

PIN No.	PIN Name	Type	Description
1	Amplifier-	Audio In/Out	Audio Amplifier Input /Output
2	Amplifier+	Audio In/Out	Audio Amplifier Input /Output

3.2 Power Socket

The MOLEX 4-pin connector provides a 12V power supply interface. The socket interface definitions are shown in Table 3.2.

Table 3.2 Pinout of 53398-0471 4-Pin Socket

PIN No.	PIN Name	Type	Description
1	DC12V	Power	Power In (12V DC)
2	DC12V	Power	Power In (12V DC)
3	GND	Power	Power GND
4	GND	Power	Power GND

3.3 Ethernet Socket

The MOLEX 8-pin connector supports Ethernet and analog video interfaces. The socket interface definitions are shown in Table 3.3.

Table 3.3 Pinout of MOLEX 53398-0871 8-Pin Socket

PIN No.	PIN Name	Type	Description
1	ETHRX+	Signal In	Megabit Network Differential Output
2	ETHRX-	Signal In	Megabit Network Differential Output
3	ETHTX+	Signal Out	Megabit Network Differential Input
4	GBL_RST	Input Signal	Restore Factory Settings (default high)
5	GND	Power	GND
6	ETHTX-	Signal Out	Megabit Network Differential Input
7	VGND	Power	Analog Video GND
8	CVBS	Analog Signal	Analog Video Output Signal

3.4 Functional Socket

The MOLEX 53398-1271 12-pin connector provides audio input and output, alarm input and output, and RS-485 interfaces. The socket interface definitions are shown in Table 3.4.

Table 3.4 Pinout of MOLEX 53398-1271 12-Pin Socket

PIN No.	PIN Name	Type	Description
1	MIC+	Signal In	MIC Differential Input
2	MIC-	Signal In	
3	LINE_OUT	Signal Out	Audio Signal Output
4	LINE_GND	Signal GND	Audio Signal Output GND
5	/	/	/
6	RS485+	In/Out	RS485 Signal Input/Output
7	RS485-	In/Out	
8	ALARMIN1	Signal In	Alarm Signal Input
9	ALARMIN2	Signal In	
10	GND	Power	Power GND
11	ALMOUT+	Signal Out	Alarm Signal Output
12	ALMOUT-	Signal Out	

3.5 Serial Port Socket

The MOLEX 3-pin connector supports a UART serial communication interface. The socket interface definitions are shown in Table 3.5.

Table 3.5 Pinout of MOLEX 53398-0371 3-Pin Socket

PIN No.	PIN Name	Type	Description
1	UART_RX	Signal Out	Serial Port Signal Input (+3.3V)
2	UART_TX	Signal In	Serial Port Signal Output (+3.3V)
3	GND	Power	GND

4. Introduction of Digital Video Format

4.1 LVCMOS Video Format

The LVCMOS digital video signals contain one clock signal (Clock), one frame valid signal, one line valid signal, fourteen data signals (DV0-DV13). When one frame data comes, the frame synchronizing signal is set high level, which indicates that the following data belongs to the same frame. After this frame data is finished, the frame synchronizing signal is set low level, which indicates that this frame data is finished; For the same reason, when one line data comes, the line synchronizing signal is set high level, after this line of data is finished, the line synchronizing signal is set low level. Refer to the following Figure 4.1 for the sequence chart of LVCMOS video:

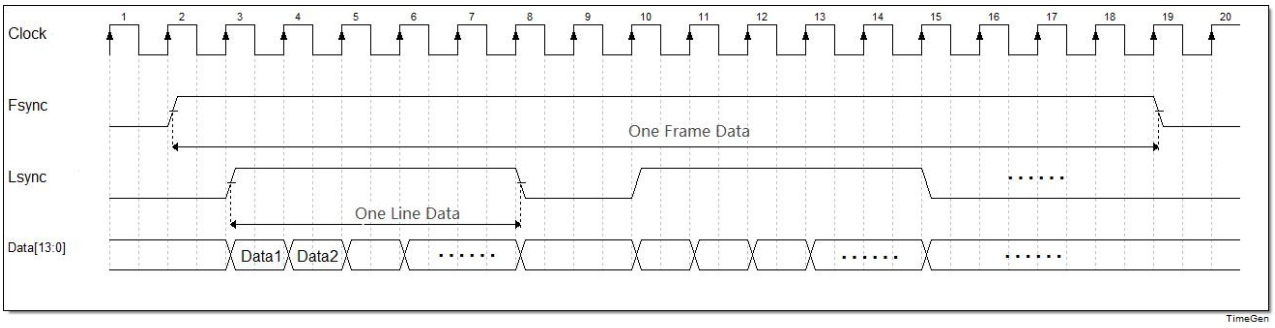

Figure 4.1 LVCMOS Timing

Users can choose the ORG(original) data, NUC(Non-uniformity Correction) data, DNS(image denoising) data and DRC(image processing) data for LVCMOS data source. For the above data source, except that every pixel for DRC data is 8bit, the pixel for other data sources is 14 bit; in the above figure, the synchronizing signal and data signal are all changed on the clock rising edge. In order to make sampling on the rising edge of clock, the signal can be changed on the falling edge of the clock in actual program design.

Table 4.1 LVCMOS CLK Frequency

Model	CLK Frequency
F640	37.5 MHz
F384	45 MHz

4.2 BT.1120 Video Format

There are two kinds of BT.1120 digital video timing for uncooled thermal imaging cores, internal sync and external sync. Internal sync adopts sync reference number to indicate the start and end of every line or every frame, 16 data lines and one clock line are included. Besides 16 data lines and one clock line in

external sync, one line sync signal and one field sync signal are also included. The default BT1120 video source is DRC and it can not be changed.

For BT.1120 of uncooled thermal imaging cores, both internal sync and external sync are included, that is, the output data contains sync reference number, line sync signal and field sync signal. The data is changed during the falling edge of clock signal to ensure that the rising edge of clock is corresponding to the stable data. The video size of 640 thermal camera is 640- column, 512-row; the video size of 384 thermal camera is 384-column, 288-row.

4.2.1 Timing Introduction of External Sync

See the following Figure 4.2 for timing chart of external sync:

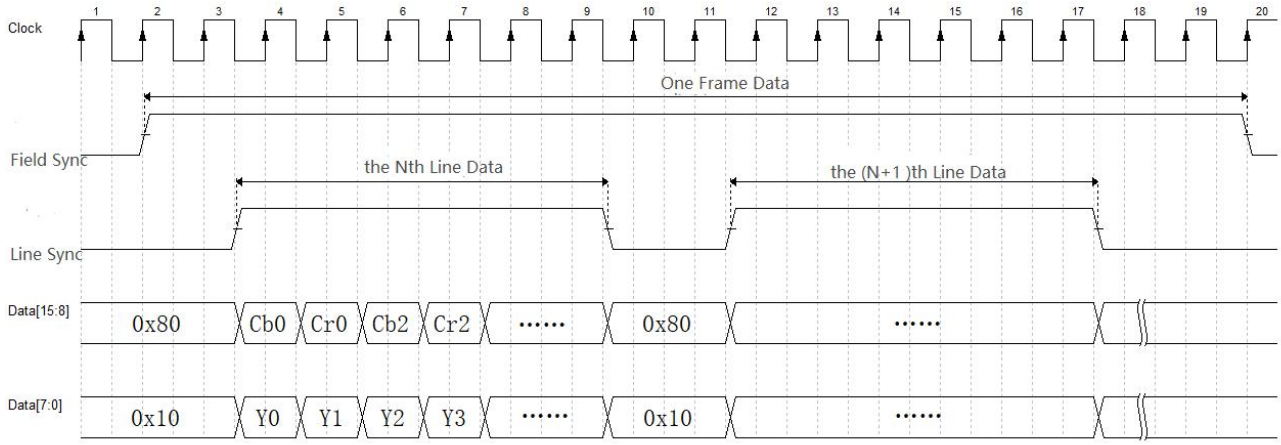

Figure4.2 Timing Chart of BT.1120 External Sync Output

16bit data (high 8bit is chroma data, low 8bit is gray data) is output in the corresponding position of line sync signal. The data output is 0x8010 when the line sync signal is 0.

4.2.2 Timing Introduction of Internal Sync

The reference number is adopted to indicate the start and end of the line or frame in internal sync, see the following Table 4.2 for the time sequence of one frame image:

Table4.2 Timing Chart of BT.1120 Internal Sync Output

Invalid line reference code EAV	Blanking 0x8010	Invalid line reference code SAV	Blanking 0x8010
Valid line reference code EAV	Blanking 0x8010	Valid line reference code SAV	Valid data Area The data area size of 640 thermal camera is 640*512
Invalid line reference code EAV	Blanking 0x8010	Invalid line reference code SAV	Blanking 0x8010

The above Table describes format of one frame image which includes valid line, invalid line, blanking and valid data area. The top left corner stands for start of a frame, the bottom right corner stands for end of a frame; the size of one frame, number of invalid line and valid line, the size of blanking area, etc. is decided by the actual status of the thermal camera. All the data in blanking area is 0x8010, every reference number is corresponding to 4 clock periods, and every pixel data is corresponding to one clock period. The reference number and pixel data are all 16bit, see Table 4.3 for the format of the reference code:

Table 4.3 Reference Code Format

	EAV	SAV
Invalid Line	0xFFFF 0x0000 0x0000 0xB6B6	0xFFFF 0x0000 0x0000 0xABAB
Valid Line	0xFFFF 0x0000 0x0000 0x9D9D	0xFFFF 0x0000 0x0000 0x8080

For 16bit data, high 8bit is chroma data, low 8bit is gray data in internal sync. The first three clock period of every reference number are 0xFFFF, 0x0000, 0x0000.

Table4.4 BT.1120 CLK Frequency

Model	CLK Frequency
F640	37.5MHz
F384	45MHz

4.3 BT.601 Video Format

The BT.601 digital video timing for the thermal imaging cores can be configured in two ways: internal synchronization and external synchronization. The internal synchronization method uses a synchronization reference code to indicate the start and end of data for each line or frame, comprising 8 data lines and one clock line. The external synchronization method includes 8 data lines, one clock line, a line synchronization signal, and a frame synchronization signal. The BT.601 digital video source defaults to DRC and is not changeable.

The BT.601 video output from the uncooled thermal imaging cores includes both internal and external synchronization. In other words, the data output via the 8 data lines contains synchronization reference codes and also provides line synchronization and frame synchronization signals. Furthermore, the data transitions are synchronized with the falling edge of the clock signal to ensure that the rising edge of the clock at the receiver corresponds precisely to stable data. For a 640-core output, the video dimensions are 640 columns by 512 rows, and for a 384-core output, the video dimensions are 384 columns by 288 rows.

4.3.1 Timing Introduction of External Sync

See the following Figure 4.3 for timing chart of external sync, for 640 array format, 640*2 clocks are output in a line of data:

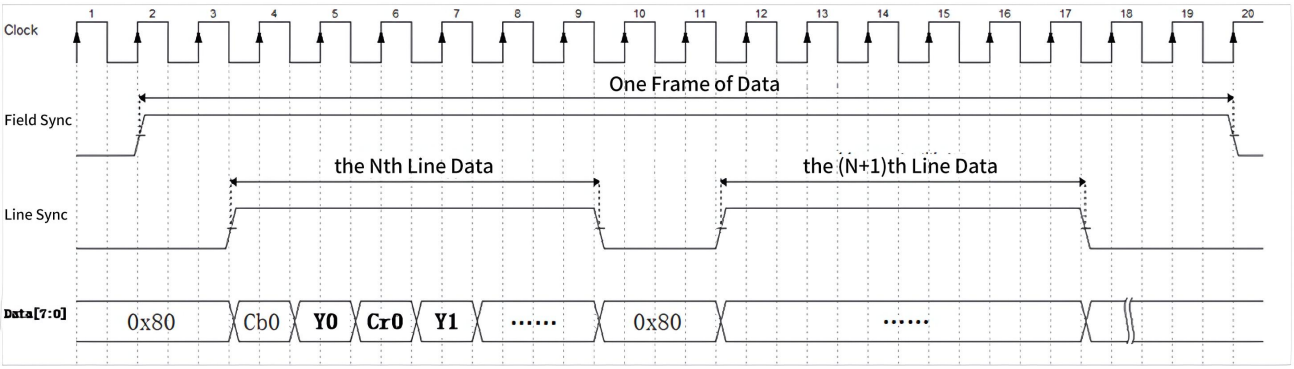

Figure 4.3 Timing Chart of BT.601 External Sync Output

4.3.2 Timing Introduction of Internal Sync

The reference number is adopted to indicate the start and end of the line or frame in internal sync, see the following Table 4.5 for the timing of one frame image:

Invalid line reference code EAV 0xB6B6	Blanking 0x8010	Invalid line reference code SAV 0xABAB	Invalid data 0x8010
Valid line reference code EAV 0x9D9D	Blanking 0x8010	Valid line reference code SAV 0x8080	Valid data Area Cb Y Cr Y The data area size of 640 thermal imaging core is 640*512*2
Invalid line reference code EAV 0xB6B6	Blanking 0x8010	Invalid line reference code SAV 0xABAB	Invalid data 0x8010

The above table represents the format of a single frame of an image. A frame of an image consists of invalid lines, valid lines, a blanking region, and a valid data region. The top-left corner of the table corresponds to the start of a frame, and the bottom-right corner corresponds to the end of a frame. The invalid lines at the top and bottom have a size of only 1 line. Both the blanking region and the invalid data have a content of 0x8010. The specific format of one line of video data is described in the table below.

Table 4.6 Line Data Format of BT.601

	EVA Reference Code				Blanking				SAV Reference Code				Data							
													Image							
Byte Count	4 Bytes				---				4 Bytes				640*2 Bytes							
	FF	00	00	EVA	Cb	Y	Cr	Y	FF	00	00	SAV	Cb	Y	Cr	Y	Cb	Y	Cr	Y
Invalid Line	FF	00	00	B6	80	10	80	10	FF	00	00	AB	80	10	80	10	80	10	80	10
Valid Line	FF	00	00	9D	80	10	80	10	FF	00	00	80	U	Y	V	Y	U	Y	V	Y

Table 4.7 BT.601 CLK Frequency

Model	CLK Frequency
F640	37.5MHz
F384	45MHz

4.4 CDS_2 Video Format

The CDS_2 video adds temperature data on the basis of BT1120, it can output image data and temperature data at the same time. The output image is totally the same with BT1120 in CDS_2 video, but in CDS_2 image data, the high 8bit is brightness Y, low 8bit is chroma CbCr, which is contrary to BT1120. The format of CDS_2 video is very similar to Bt1120, it just adds temperature data in effective data. The CDS_2 video needs one CLK line, one fsync line, one lsync line and 16 data lines, the high level is 3.3V, the low level is 0V. The highest 2bit outputs low level in 16bit data while outputting temperature data.

See the following table for the video format of CDS_2 video:

Table 4.8 CDS_2 Frame Data Format

Reference code of invalid line EAV 0xB6B6	Blanking Area 0x1080	Reference code of invalid line SAV 0xABAB	Invalid Data 0x1080	
Reference code of valid line EAV 0x9D9D	Blanking Area 0x1080	Reference code of valid line SAV 0x8080	Image data in valid data area YCbYCr 640*512	Temperature data in valid data area 14bit 640*512
Reference code of invalid line EAV 0xB6B6	Blanking area 0x1080	Reference code of invalid line SAV 0xABAB	invalid data 0x1080	

The internal sync code of the CDS_2 video is totally the same with that of BT1120. There are both internal sync and external sync for CDS_2 video, there are line sync signals and frame sync signals besides clk signals and data signals. The high level length of line sync signal for CDS_2 video is two times than that of BT1120, and the high 8bit of the 16bit image data is brightness Y, low 8bit is chroma CbCr, and the blanking area and the invalid data area is 0x1080 instead of 0x8010.

The time sequence format of CDS_2 with valid data is as follows.

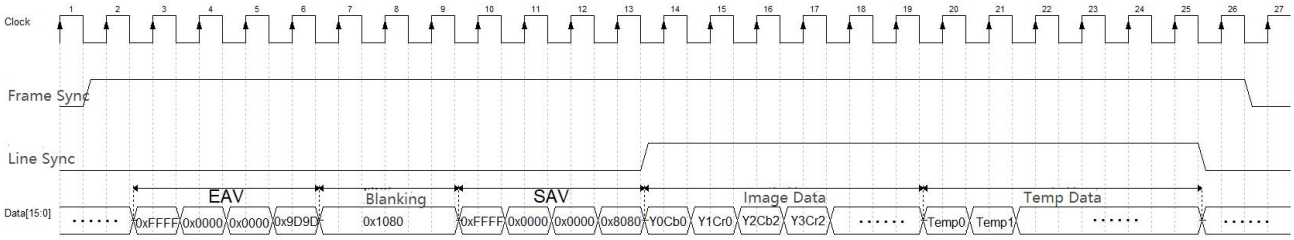

Figure 4.4 Timing of CDS_2

Table 4.9 CDS_2 CLK Frequency

Model	CLK Frequency
F640	37.5MHz
F384	45MHz

4.5 CDS_3 Video Format

CDS_3 video is based on BT601 video and incorporates temperature data. It can simultaneously output image data and temperature data. CDS3 video does not require frame synchronization signals or line synchronization signals; it only needs one clock signal and eight data lines. CDS3 video data is arranged in a line-by-line manner. Each line of CDS3 video data includes three parts: the reference code (EAV/SAV), blanking region, and data region. Rows with valid data are considered valid lines, while rows with no valid data are invalid lines. The simplified diagram of one frame of CDS_3 video format is shown in the figure below:

Table 4.10 CDS_3 Frame Data Format

<table>
<tr><td>EAV reference code of invalid line</td><td>Blanking Area
0x80 0x10</td><td>SAV reference code of invalid line</td><td colspan="2">Invalid Data
0x80 0x10</td></tr>
<tr><td>EAV reference code of valid line</td><td>Blanking Area
0x80 0x10</td><td>SAV reference code of valid line</td><td>Valid Image data
640*512
pixel/640*512*2 clk</td><td>Valid temperature data
640*512
pixel/640*512*2 clk</td></tr>
<tr><td>EAV reference code of invalid line</td><td>Blanking area
0x80 0x10</td><td>SAV reference code of invalid line</td><td colspan="2">Invalid data
0x80 0x10</td></tr>
</table>

The data in the blanking region and data region are arranged in the order of Cb Y Cr Y, where Cb and Cr are the chrominance components, and Y represents the brightness component. Cb, Cr, and Y all have an 8-bit width, each corresponding to one clock cycle. A set of Cb Y Cr Y corresponds to data for two pixels, which is equivalent to four clock cycles.

For the blanking region and invalid data, the chrominance components Cb and Cr are fixed at 0x80, and the brightness component Y is fixed at 0x10. For the image region within the valid data, both the chrominance components Cb and Cr are 8 bits wide, and the brightness component Y represents an 8-bit infrared grayscale value. For the temperature region within the valid data, the chrominance components Cb and Cr are the low 8 bits of the temperature data, denoted as TEMP[7:0], and the brightness component Y represents the high 8 bits of the temperature data, denoted as TEMP[15:8].

Table 4.11 Line Data Format of CDS_3

	EVA Reference Code				Blanking Area				SAV Reference Code				Data							
													Image				Temperature			
Byte Count	4 Bytes				---				4 Bytes				640*2 Bytes				640*2Bytes			
	FF	00	00	EVA	Cb	Y	Cr	Y	FF	00	00	SAV	Cb	Y	Cr	Y	Cb	Y	Cr	Y
Invalid Data	FF	00	00	B6	80	10	80	10	FF	00	00	AB	80	10	80	10	80	10	80	10
Valid Data	FF	00	00	9D	80	10	80	10	FF	00	00	80	U	Y	V	Y	TEMP [7:0]	TEMP [15:8]	TEMP [7:0]	TEMP [15:8]

Table 4.12 CDS_3 CLK Frequency

Model	CLK Frequency
F640	37.5MHz
F384	45MHz

5. Precautions

To protect you and others from injury or to protect your equipment from damage, please read all the following information before using your equipment.

1. The product should not be made towards the sun directly and other high-intensity radiation sources;
2. The optimal environment temperature for operating is - 20 ℃ to 50 ℃;
3. Do not touch or hit the detector window with hands or other objects;
4. Do not touch the equipment and cables with wet hands;
5. Please do not bend or damage cables;
6. Do not scrub your equipment with diluents;
7. Should not unplug and plug other cables without disconnecting the power supply;
8. Wrong cable should not be connected in case that brings damages to the equipment;
9. Please pay attention to prevent static electricity;

10. Please do not disassemble the equipment. If there is any fault, please contact our company, and professional personnel will carry out maintenance.